JINGMEI LIANG

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DIELECTRIC SYSTEM & MODULE DIVISION

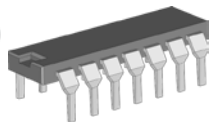
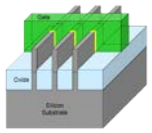
APPLIED MATERIALS®

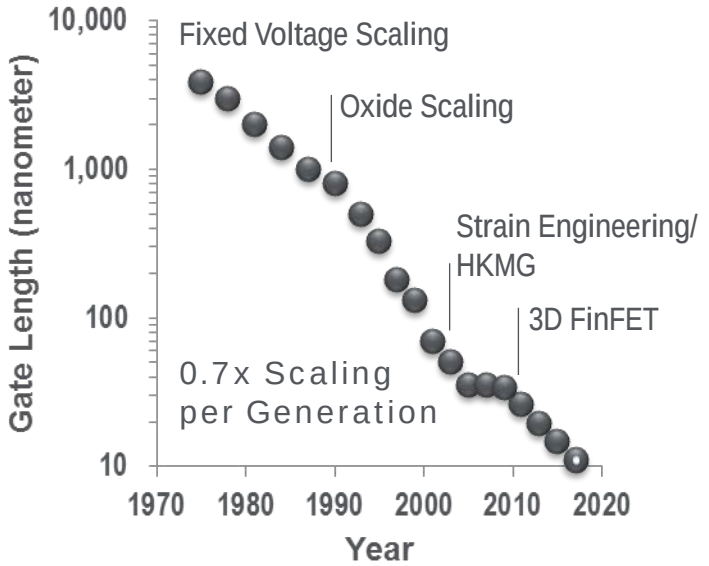
VISION: Define and transform atomic dimension research to high volume industrial production. Design chemical vapor deposition (CVD) processes & reactor chambers for advanced logic & memory chip manufacturing though small geometry (≤10nm), high aspect ratio (≥20:1) dielectric gap fill methods.

TECHNOLOGY CHALLENGE & FOCUS:

- Interoperate, enable new transistor architectures & materials
- Invent diverse gap fill dielectrics for self-aligned patterning

- *Explore & Design New Precursor Chemistry*
- *Create Deposition Method & Reactor Chamber*
- *Productize for Process Reliability & Stability*
- *Validate & Collaborate with Device Chip Makers*

	Past	Present	Future
Transistor Feature Size	10,000nm (1971) 	14nm (2015) 	≤ 5nm
Transistor Count	2,300	1,300,000,000	*(in R&D)*
Cost per 1000 Transistors	$150	$0.0003	:



Applied Materials Producer® GT System