Semiconductor Research Corporation

PIONEERS IN COLLABORATIVE RESEARCH®

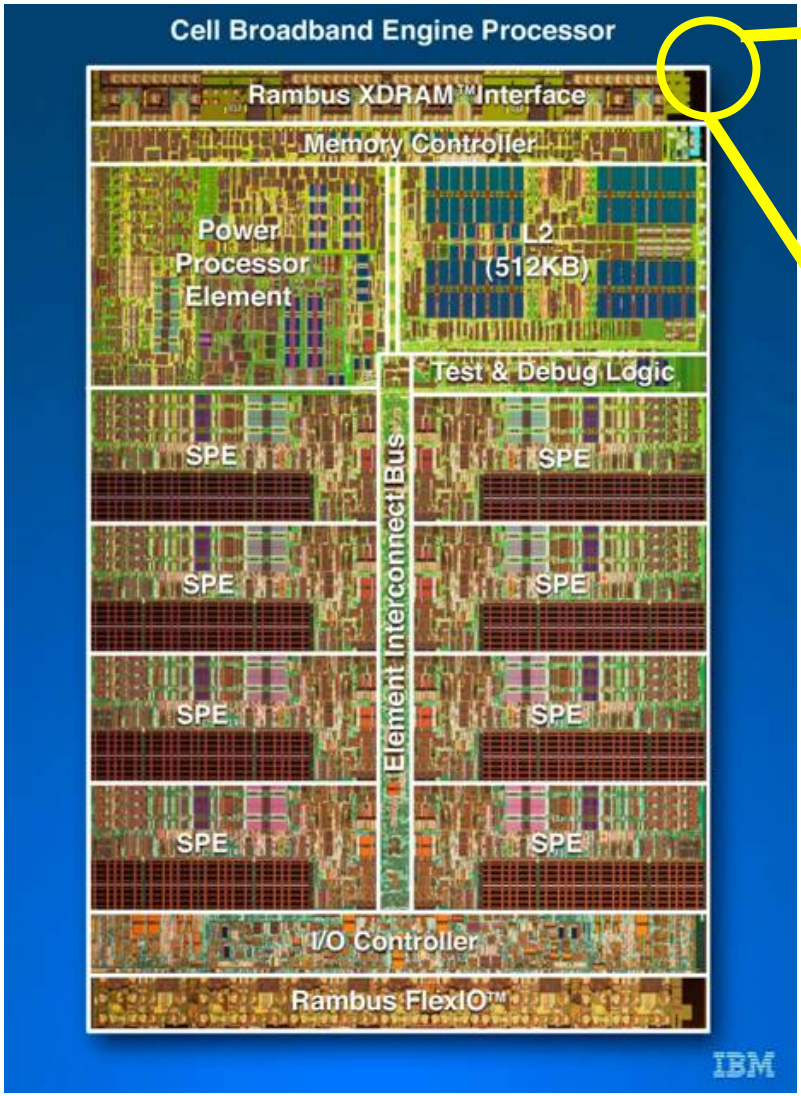
nanoelectronics RESEARCH INITIATIVE

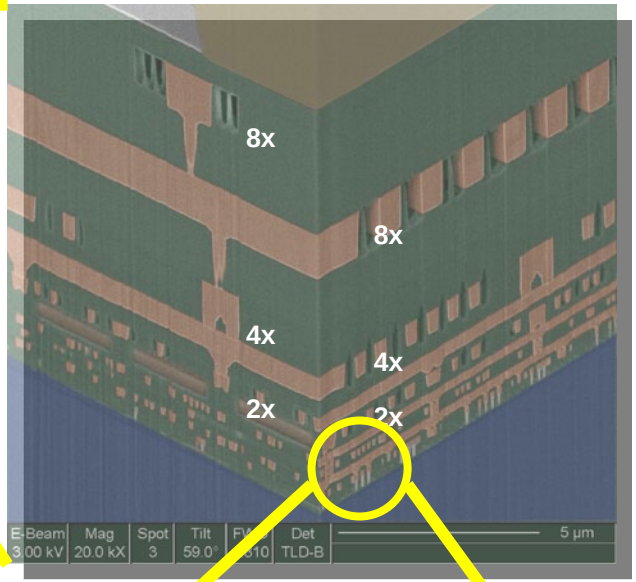
The Quest for the Next Information Processing Technology

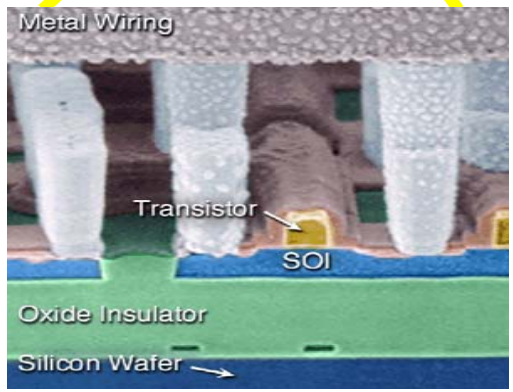
Dr. Jeff Welser
Director, SRC Nanoelectronics Research Initiative
IBM Almaden Research Center

September, 2008

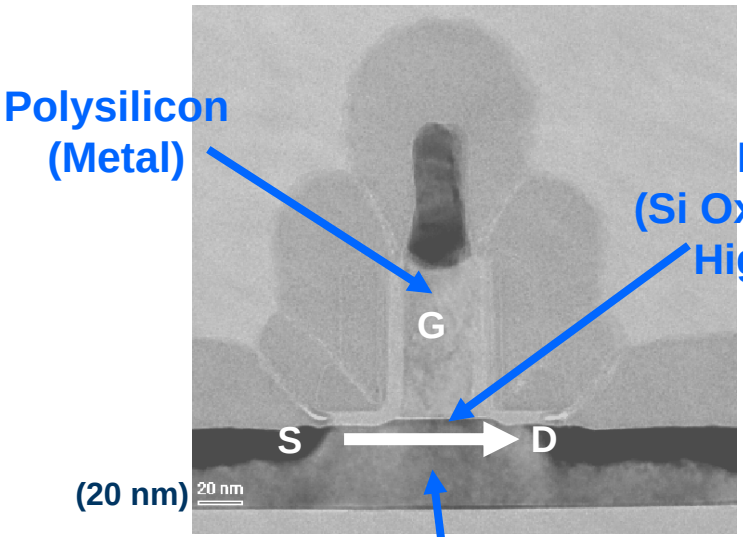
Modern IC Chip Structure

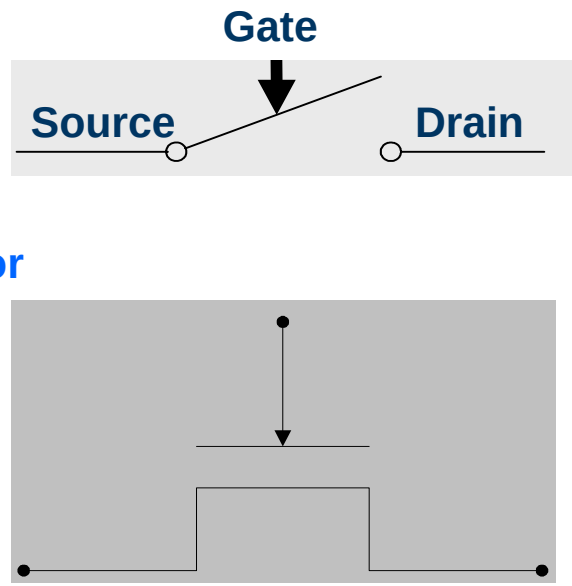






Today's Switch: CMOS-FET

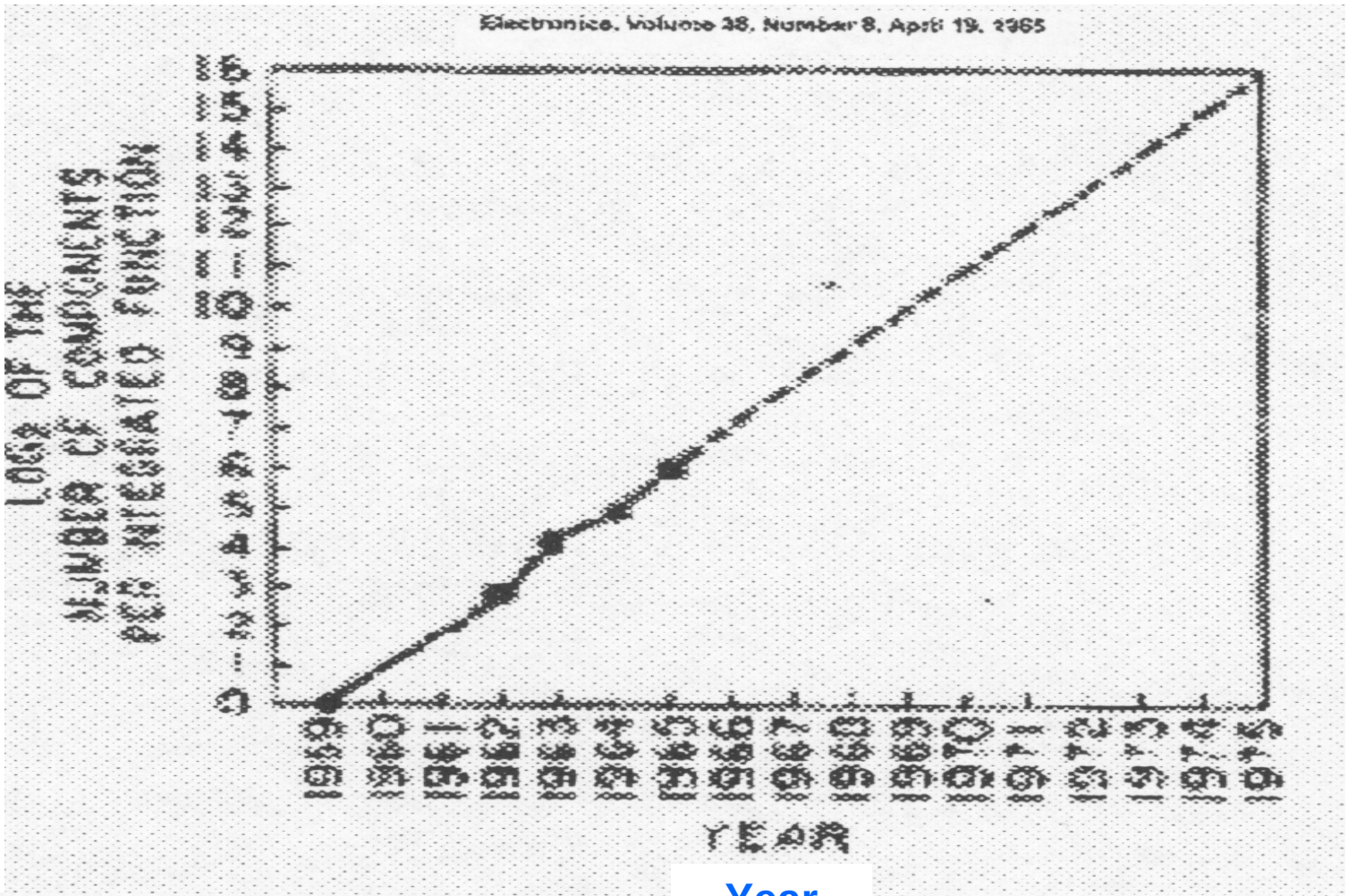




- Complementary Metal-Oxide-Semiconductor (CMOS) Field-Effect Transistor (FET)
  - N-type (electron carriers) and P-type (hole carriers) integrated together
  - Used primarily as a digital on/off switch
- Basic transistor used on digital Integrated Circuits (IC) chips
  - ~1 billion on the biggest chips today (~4 cm^2)

Moore's Law

Electronics, Volume 38, Number 8, April 19, 1965

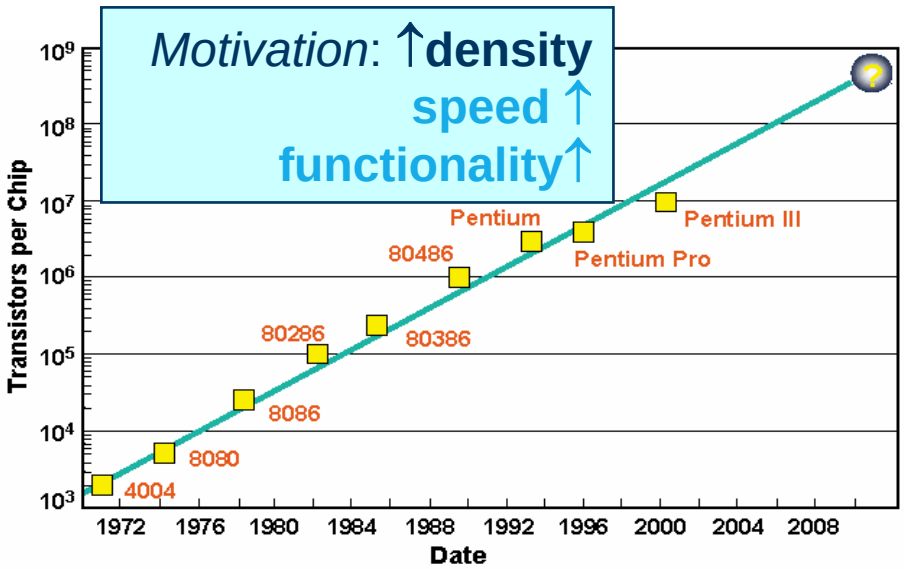


Log of the Number of Components Per Integrated Function

Year

Moore's Law: Transistors per chip

Binary Information Throughput (BIT)



Source: Stan Williams, Hewlett Packard

What is the ultimate number of binary transitions per second in a $1cm^2$ chip area?

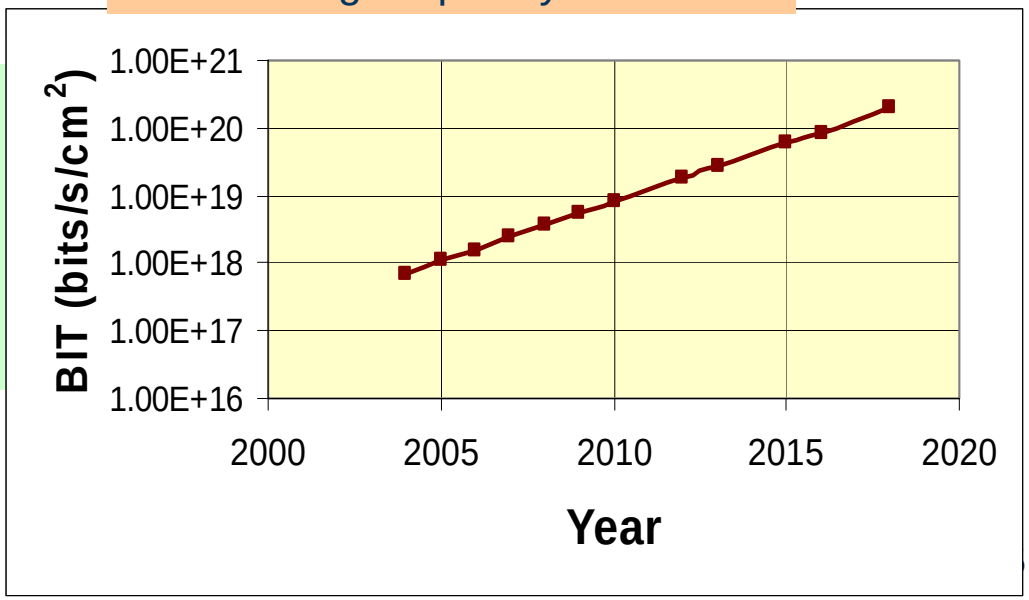
$$BIT = n_{bit} f$$

- a measure of computational capability on device level

n_{bit} – the number of binary states

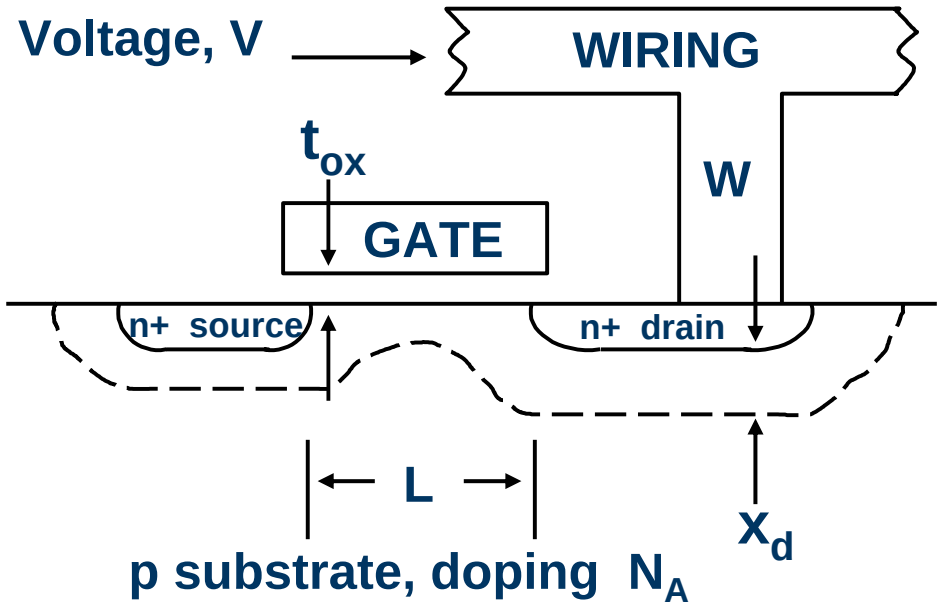
f – switching frequency

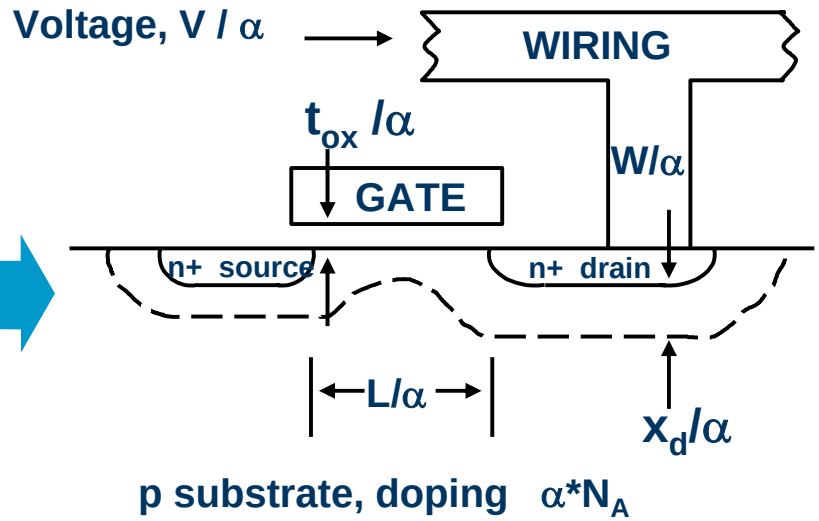
Why scaling? – To increase the *Binary Information Throughput* (BIT)

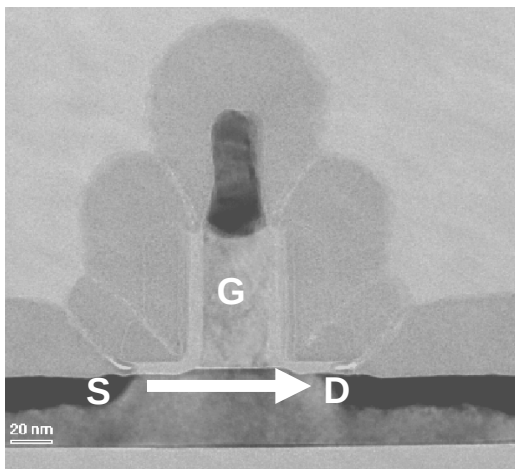


Transistor Scaling

Dennard, et al., 1974





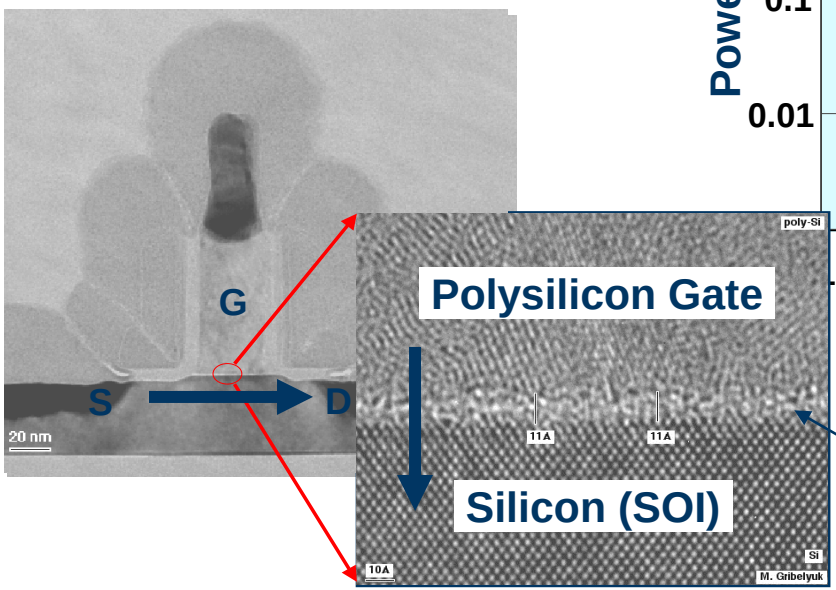


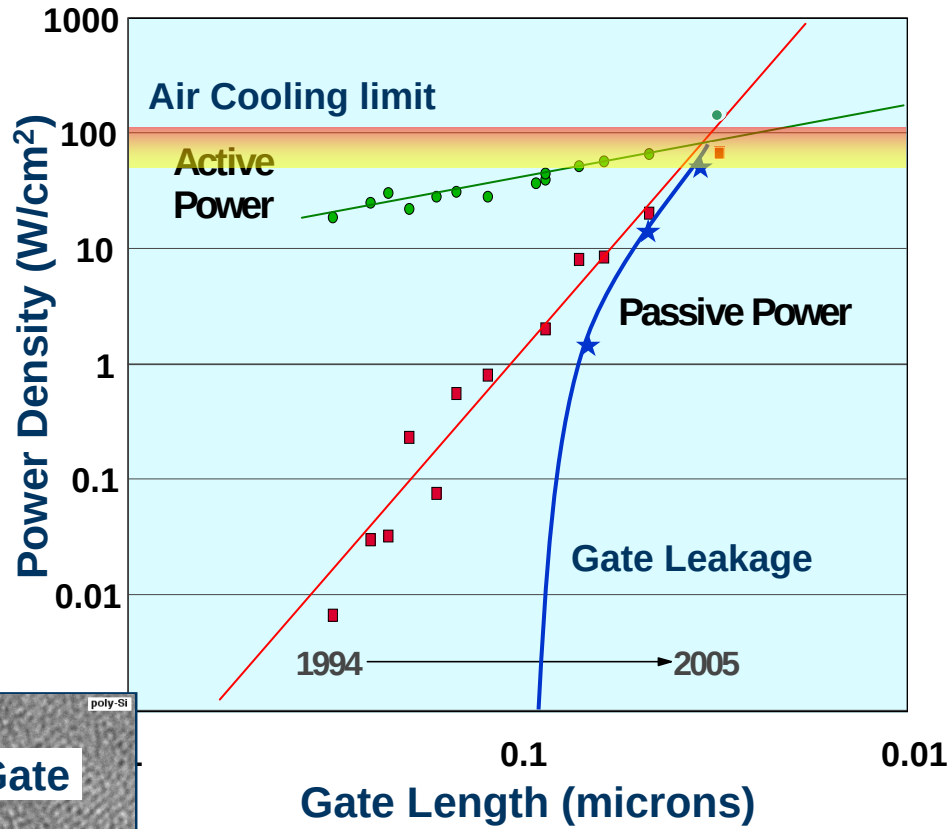
RESULTS:

Higher Density:	α^2
Higher Speed:	α
Lower Power:	$1/\alpha^2$
per circuit	
Power Density:	**Constant**

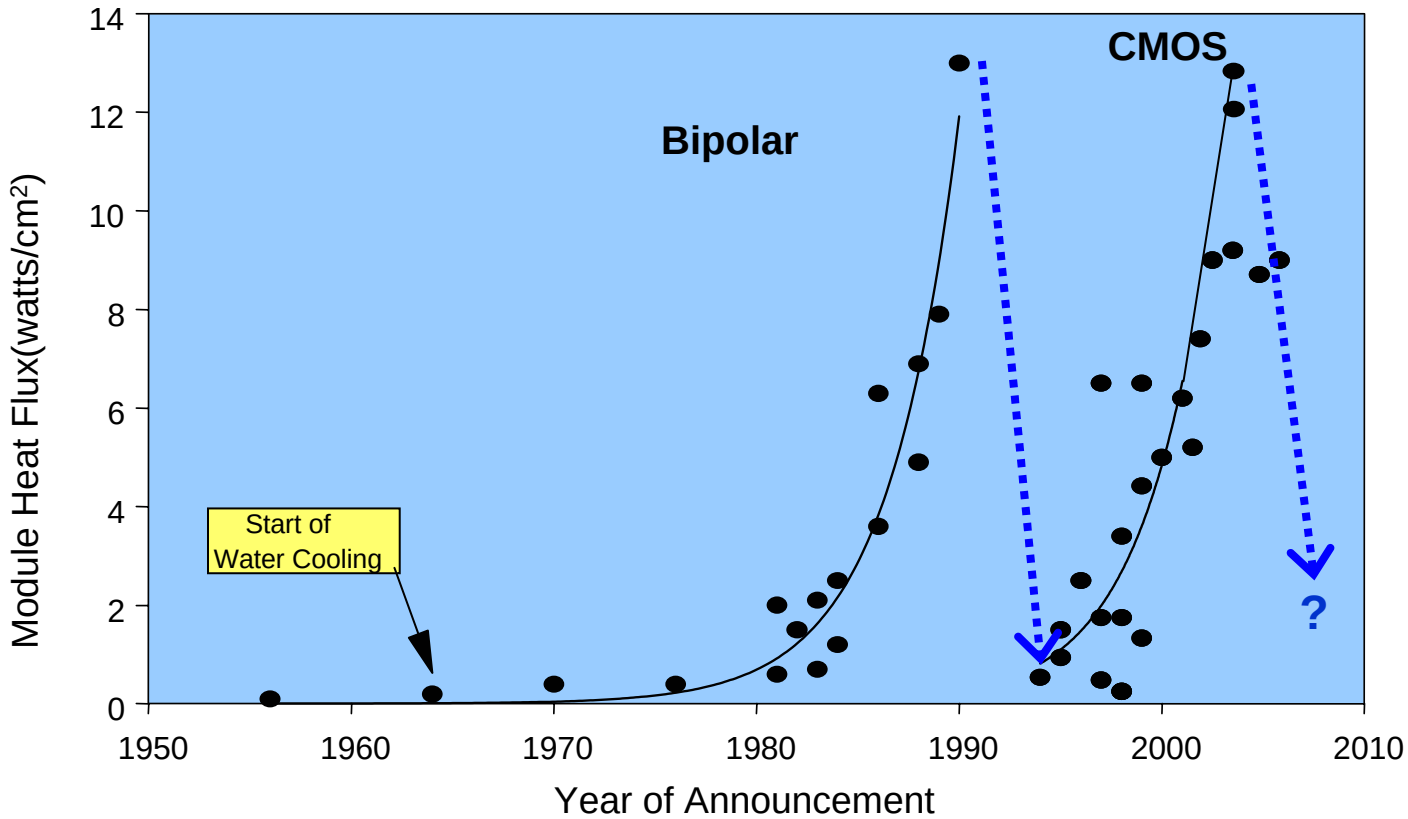
CMOS Power Issue: Active vs. Passive Power

- Power components:
  - Active power
  - Passive power
    - Gate leakage
    - Source - Drain leakage





Has This Ever Happened Before?

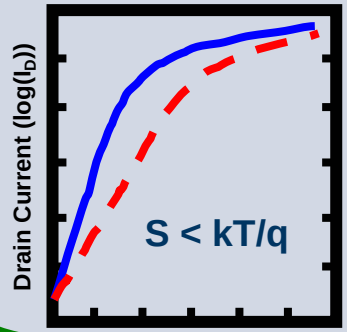


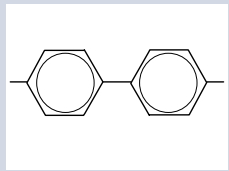
2005 ~ 2020: New utilization of technology

- Multi-core, 3D integration, new memory devices, sensors, etc.

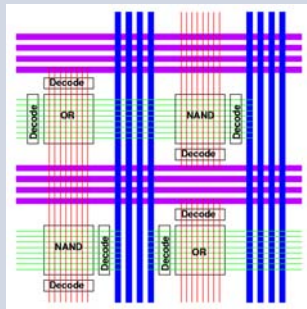
> 2020?: New technology → Nanoelectronics Research Initiative

New Device Types

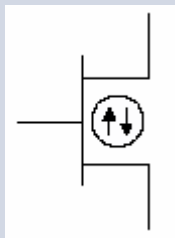




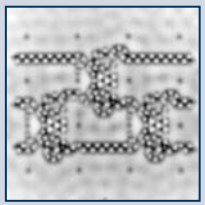
Molecular devices



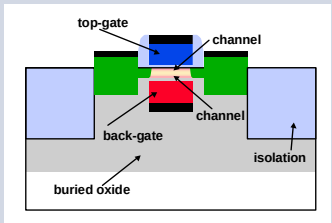
Fine-grain PLA



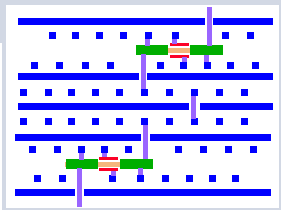
Spintronics



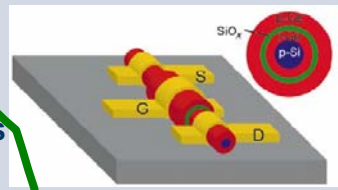
Quantum cascade



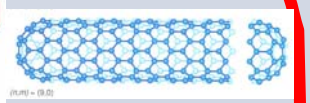
Double-Gate / FinFET



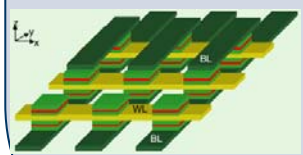
3D, heterogeneous integration

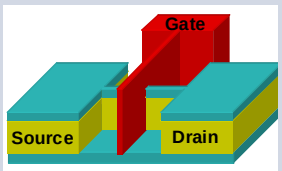


Nanowire



Nanotube

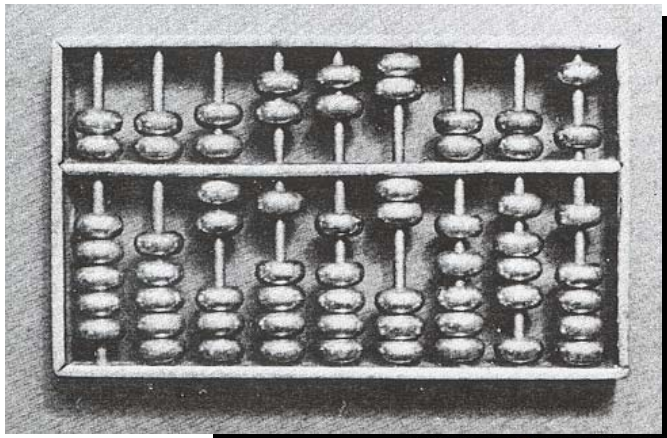




Embedded memory

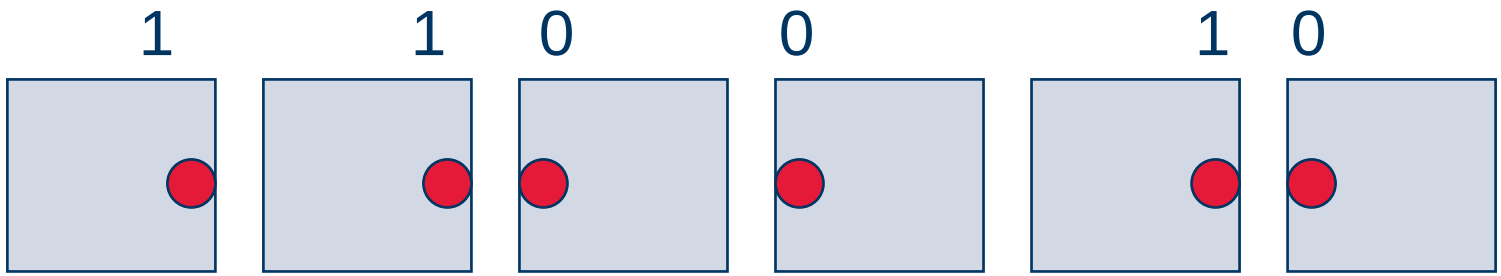
Time

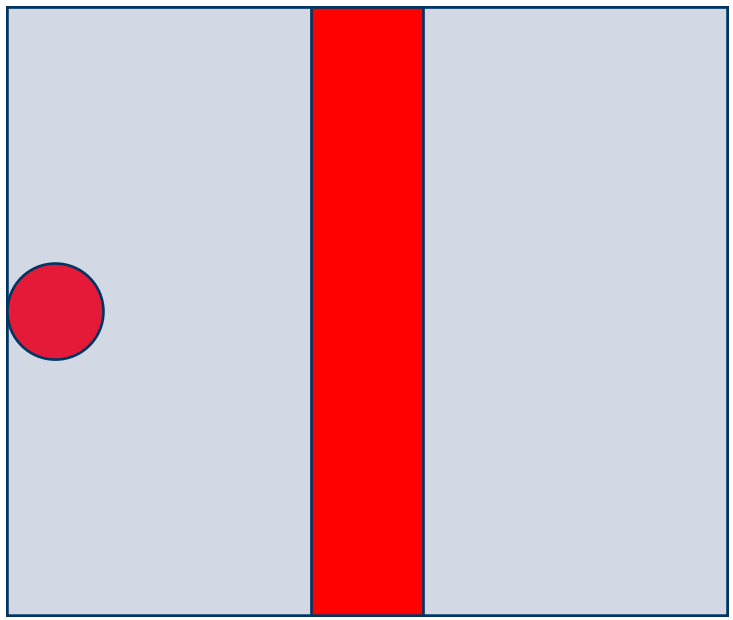
What is Information?



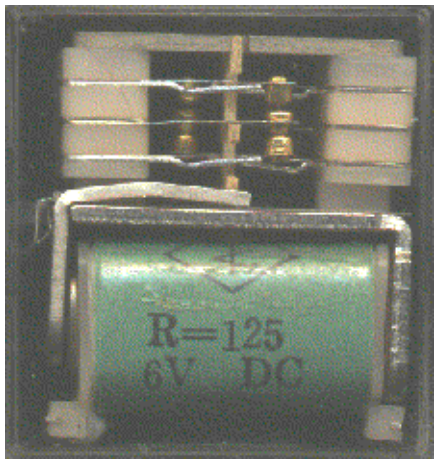
Information is measure of distinguishability manifested in physical form

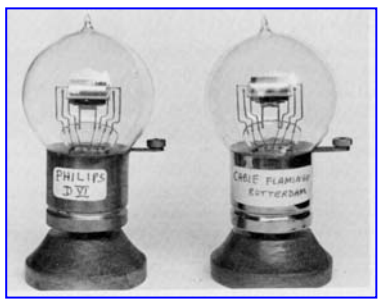
Particle Location is an Indicator of State

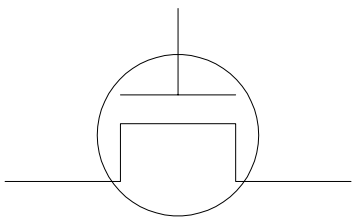




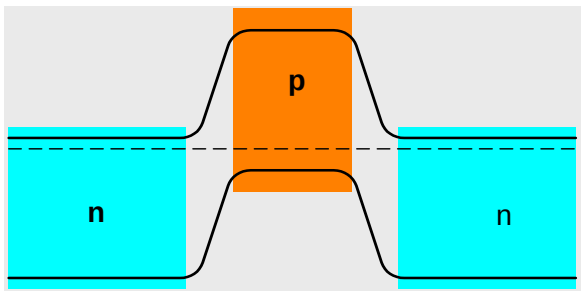
Electronic switches can be of different nature, but they all have similar fundamentals

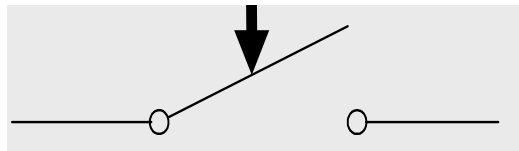


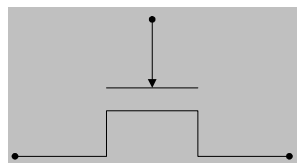


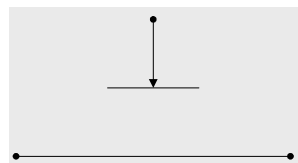


M V M

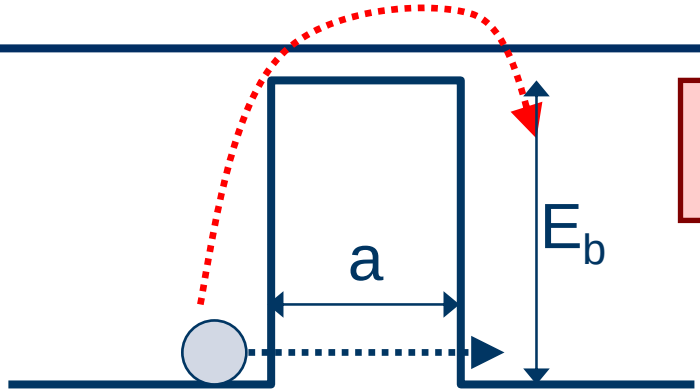




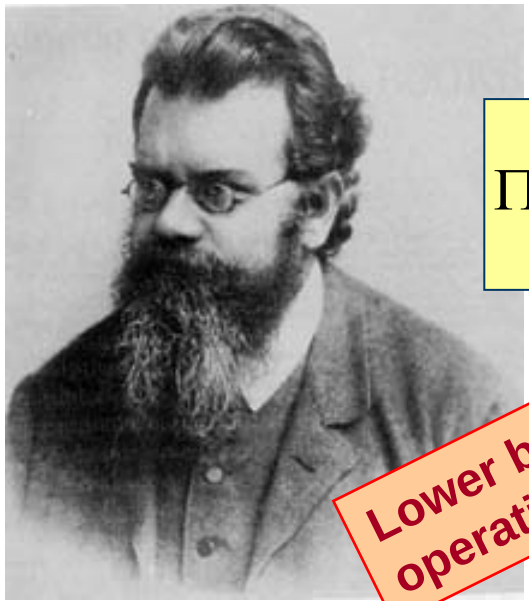




Basic Equations of Two-well Bit



What are the requirements/limitations on the height and width the barrier?



$$\Pi_B = \exp\left(-\frac{E_b}{k_B T}\right)$$

Lower bound on operation energy

“Boltzmann constraint” on minimum barrier height

$$\Delta x \Delta p \geq \hbar/2$$

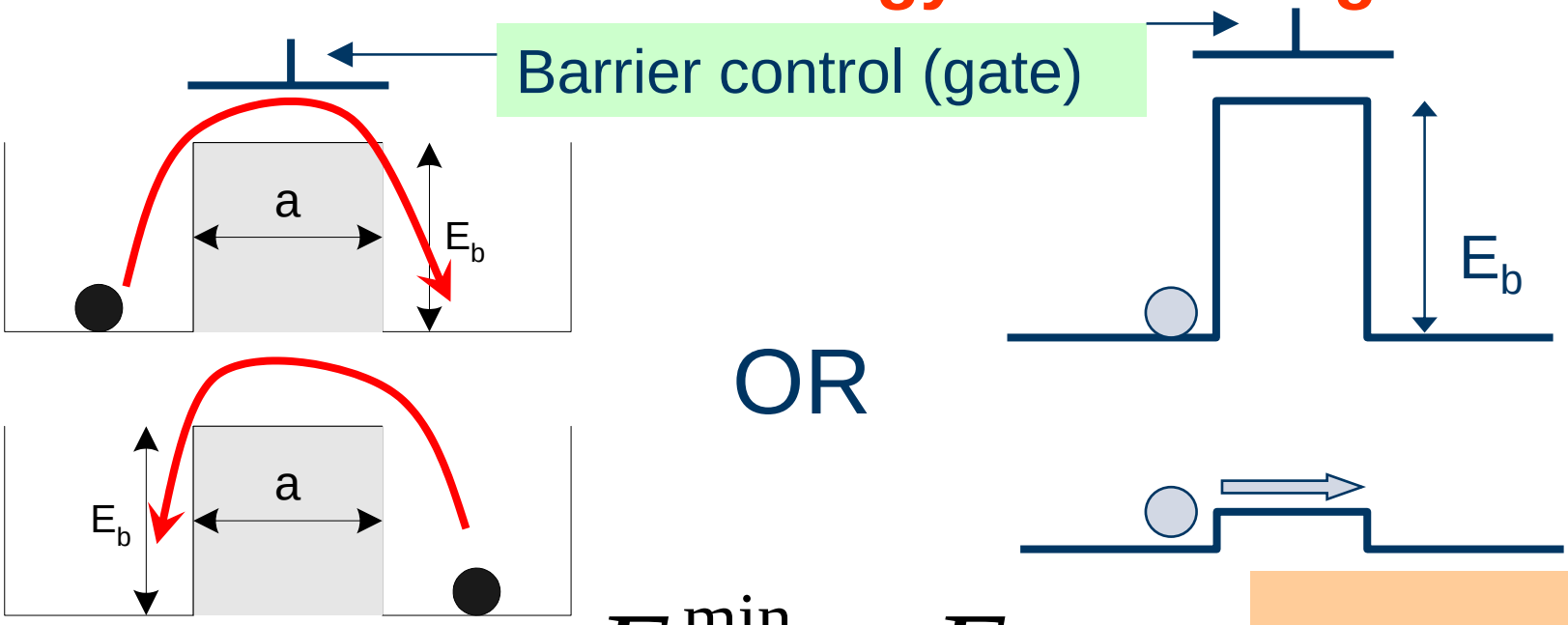
$$\Delta E \Delta t \geq h/2$$

Lower bound on device size

“Heisenberg constraints” on minimum barrier width

Classic Distinguishability:
The Boltzmann constraint

How small could the energy barrier height be ?



$$E_{bit}^{\min} = E_b$$

$$\Pi_{error} = \exp\left(\frac{E_b}{k_B T}\right)$$

$$0.5 = \exp\left(-\frac{E_b}{k_B T}\right)$$

$$E_b^{\min} = k_B T \ln 2$$

Distinguishability requirement: The probability of spontaneous transitions(errors) Π_{error}<0.5 (50%)

Energy to "deform" the barrier

Summarizing, what we have learned so far from fundamental physics

1) Minimum energy per binary transition → Boltzmann

$$E_{bit}^{\min} = k_B T \ln 2$$

2) Minimum distance between two distinguishable states

$$\Delta x \Delta p \geq \hbar$$

→ Heisenberg

$$x_{\min} = a = \frac{\hbar}{\sqrt{2mkT \ln 2}} = 1.5nm(300K)$$

3) Minimum state switching time

$$\Delta E \Delta t \geq \hbar$$

→ Heisenberg

$$t_{st} = \frac{\hbar}{kT \ln 2} = 4 \times 10^{-14} s(300K)$$

4) Maximum gate density

$$n = \frac{1}{x_{\min}^2} = 4.6 \times 10^{13} \frac{gate}{cm^2}$$

Total Power Dissipation (@E_{bit}= $kT\ln(2)$)

- A Catastrophe!

$$P_{chip} = \frac{n \cdot E_{bit}}{t} = 4.6 \cdot 10^{13}[cm^{-2}] \cdot \frac{3 \cdot 10^{-21}[J]}{4 \cdot 10^{-14}[s]}$$

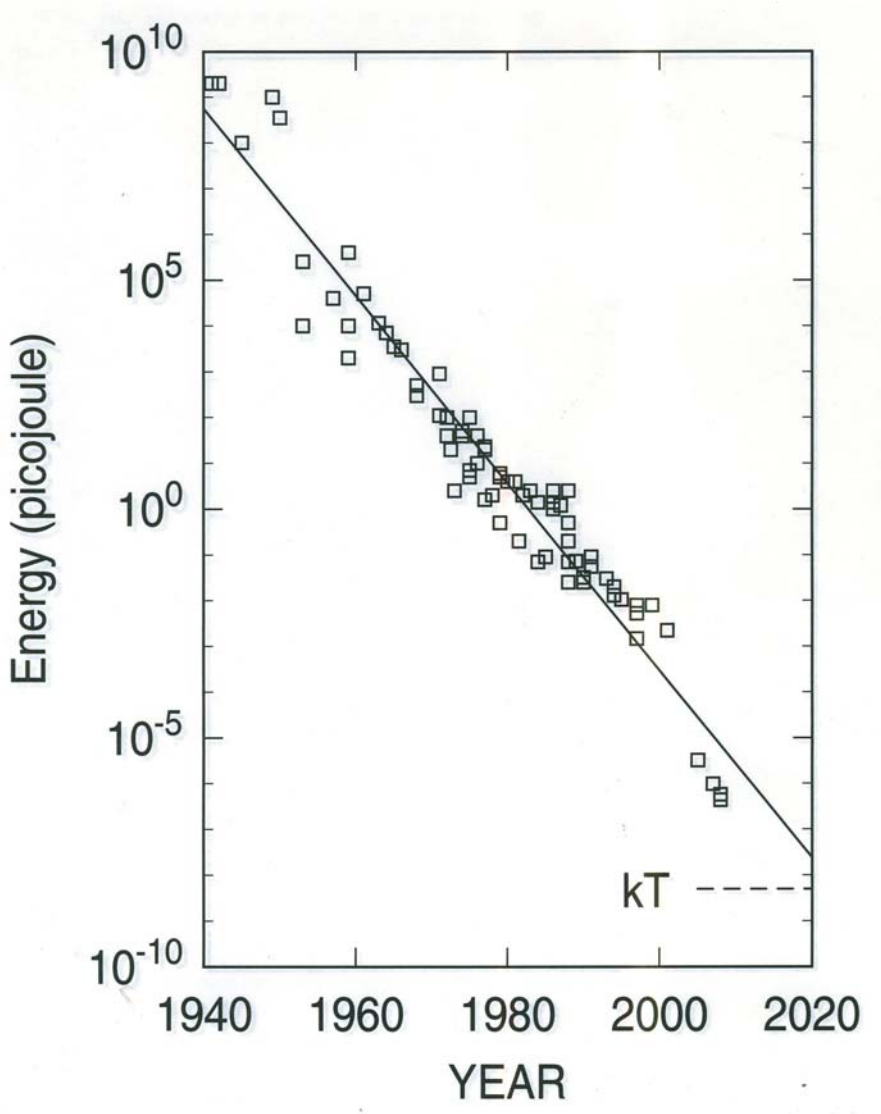
$$E_{bit} = k_B T \ln 2 \approx 3 \cdot 10^{-21}\, J$$

$$P_{chip} = 4.74 \times 10^{6} \frac{W}{cm^2}$$

T=300 K

The circuit would vaporize when it is turned on!

FETs approach the “kT” limit



Data compiled by
R. Keyes,
IBM Research Emeritus

Devices for Nanoelectronics Circuits

- **Power / Heat Generation is the main limiting factor for scaling of device speed and switch circuit density**
- Scaling to molecular sizes may not yield performance increases
  - Forced to trade-off between speed and density
- Optimal dimensions for electronic switches should be ~5-50nm
  - Achievable with Si – easily within the scope of ITRS projections
- Going to other materials for FETs will likely achieve only "one-time" percentage gains

➢ ***Need a new device mechanism or computation architecture to enable a new scaling path***

Beyond CMOS Logic: What to look for?

- To beat the power problem requires:
  - A device with a lower energy, room temperature switching mechanism

    or
  - A system that operates out of equilibrium or recovers operation energy as part of the logic computation

- **Required characteristics:**
  - **Scalability**
  - **Performance**
  - **Energy efficiency**
  - **Gain**
  - **Operational reliability**
  - **Room temp. operation**

- **Preferred approach:**
  - **CMOS process compatibility**
  - **CMOS architectural compatibility**

Alternative state variables

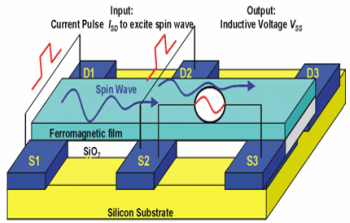
- Spin–electron, nuclear, photon
- Phase
- Quantum state
- Magnetic flux quanta
- Mechanical deformation
- Dipole orientation
- Molecular state

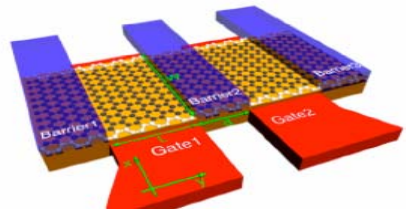
Nanoelectronics Research Initiative Mission

- **NRI Mission: Demonstrate novel computing devices capable of replacing the CMOS FET as a logic switch in the 2020 timeframe.**
  - These devices should **show significant advantage over ultimate FETs** in power, performance, density, and/or cost to enable the semiconductor industry to **extend the historical cost and performance trends** for information technology.
  - To meet these goals, NRI pursues five research vectors:
    - Device with alternative state vector
    - Non-equilibrium systems
    - Non-charge data transfer (interconnects)
    - Nanoscale phonon engineering for thermal management
    - Directed self-assembly of these new devices
  - Finally, it is desirable that these technologies be **capable of integrating with CMOS**, to allow exploitation of their potentially complementary functionality in heterogeneous systems and to enable a smooth transition to a new scaling path.

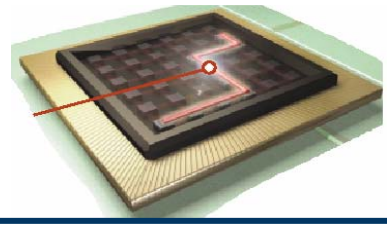
NRI Primary Research Vectors

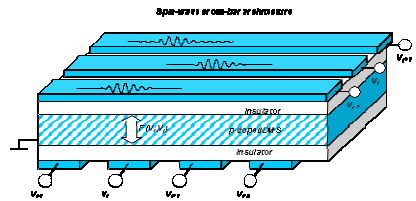
- **NEW DEVICE**
  Device with alternative state vector



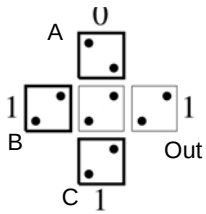


- **NEW WAYS TO CONNECT DEVICES**
  Non-charge data transfer

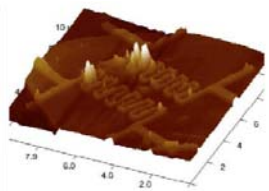




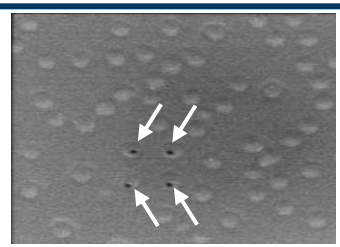
- **NEW METHODS FOR COMPUTATION**
  Non-equilibrium systems



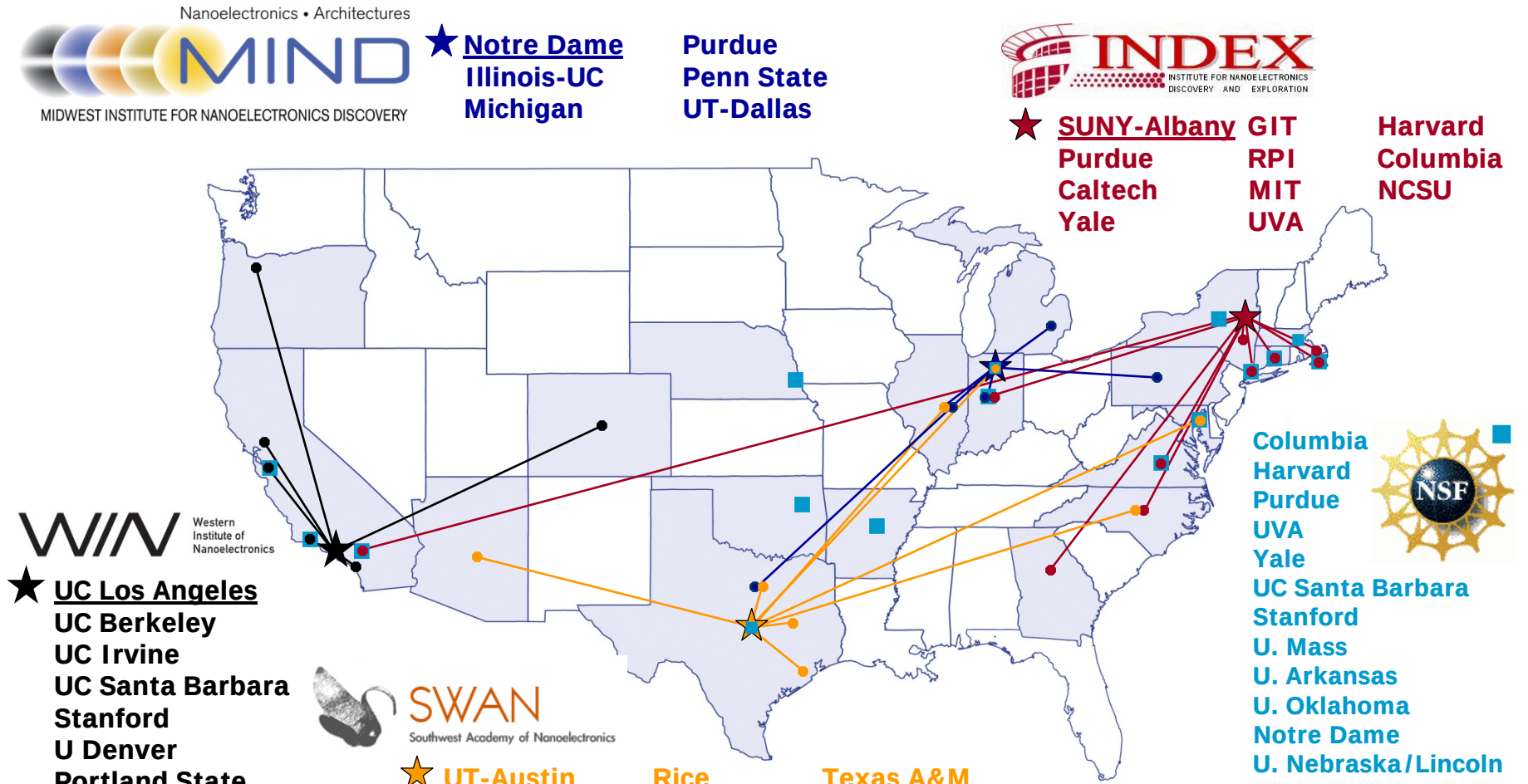
- **NEW METHODS TO MANAGE HEAT**
  Nanoscale phonon engineering



- **NEW METHODS OF FABRICATION**
  Directed self-assembly devices



NRI Funded Universities



Over 30 Universities in 19 States

NRI Research Centers

- Leveraging industry, university, and both state & fed government funds, and driving university nanoelectronics infrastructure

Western Institute of Nanoelectronics

INDEX INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

SWAN Southwest Academy of Nanoelectronics

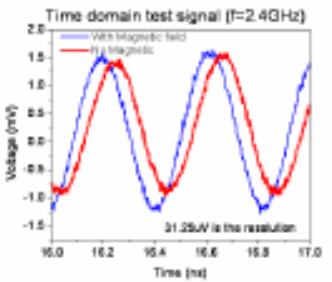
Nanoelectronics • Architectures MIND MIDWEST INSTITUTE FOR NANOELECTRONICS DISCOVERY

WIN Western Institute of Nanoelectronics	**INDEX** Institute for Nanoelectronics Discovery & Exploration	**SWAN** SouthWest Academy for Nanoelectronics	**MIND** Midwest Institute for Nanoelectronics Discovery
UCLA, UCSB, UC-Irvine, Berkeley, Stanford, U Denver, Portland State	**SUNY-Albany**, GIT, RPI, Harvard, MIT, Purdue, Yale, Columbia, Caltech, NCSU, UVA	**UT-Austin**, UT-Dallas, TX A&M, Rice, ASU, Notre Dame, Maryland, NCSU, Illinois-UC	**Notre Dame**, Purdue, Illinois-UC, Penn State, Michigan, UT-Dallas
Theme 1: Spin devices Theme 2: Spin circuits Theme 3: Benchmarks & metrics Theme 4: Spin Metrology	Task I: Novel state-variable devices Task II: Fabrication & Self-assembly Task III: Modeling & Arch Task IV: Theory & Sim Task V: Roadmap Task VI: Metrology	Task 1: Logic devices with new state-variables Task 2: Materials & structs Task 3: Nanoscale thermal management Task 4: Interconnect & Arch Task 5: Nanoscale characterization	Theme 1: Energy Efficient Devices Theme 2: Energy Efficient Architectures

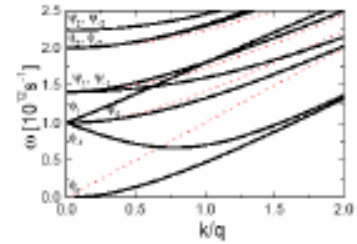
Spin Wave Device Research

Multiple PI's

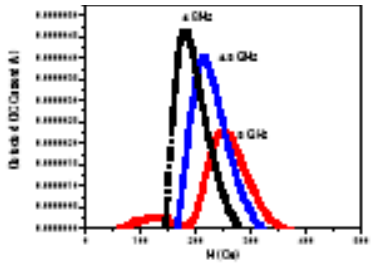
Western Institute of Nanoelectronics



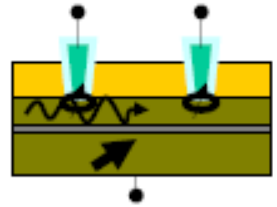
Modulation of spin wave by magnetic field



Simulation of spin wave generation by electric field (UC Berkeley)

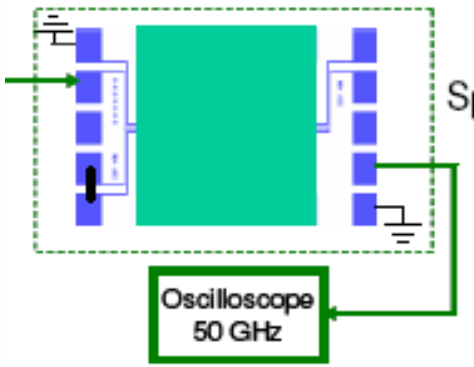


Demonstration of Spin Rectification via spin valve (UCLA)

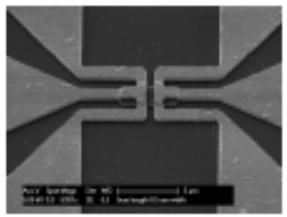


Spin Wave amplification (Staford)

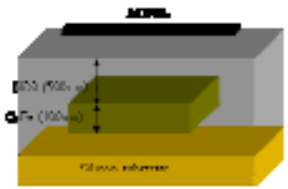
2006 → **2007** → **2008/09**



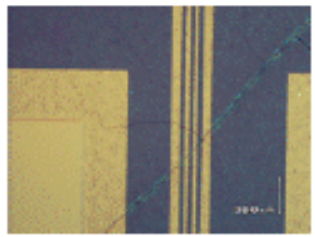
Established spin wave characterization



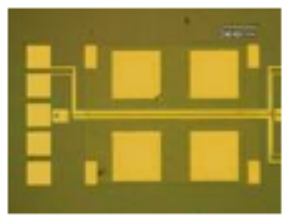
Spin Waveguides (UCSB)



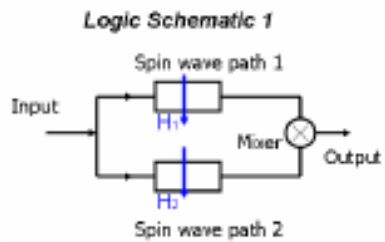
Design spin wave devices and gates



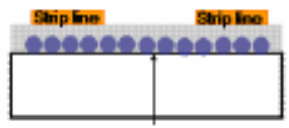
Fabricated structures using PZT and BFO



Structures to reduce Eddy Currents

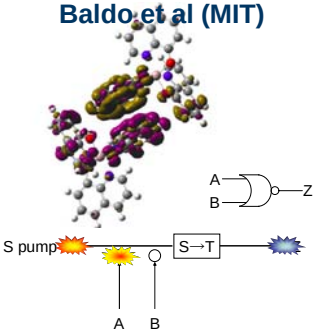


Spin wave circuits (UCSB/UCLA)

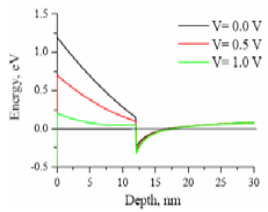


Optimize spin wave device

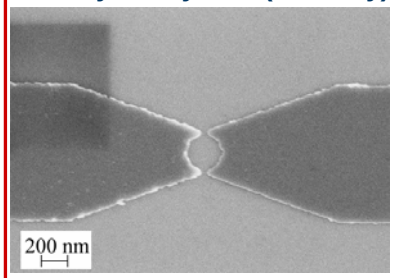
Molecular Excitons Spintronics
Baldo et al (MIT)



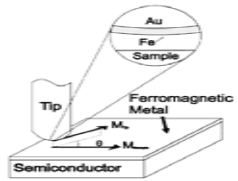
Quantum Dot Modeling
Shur et al (RPI)



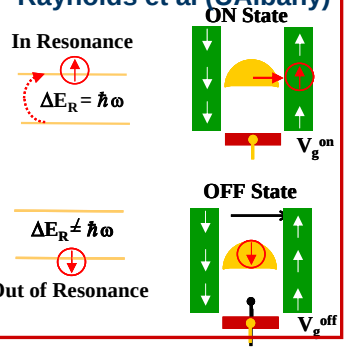
Quantum Dot Devices
Oktyabrsky et al (UAlbany)



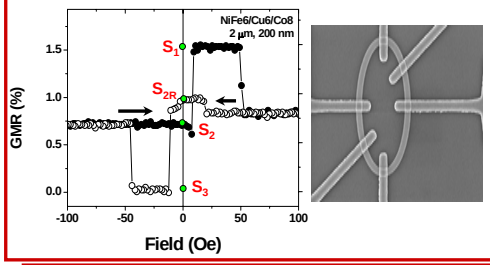
Ballistic Spin Devices
Labella et al (UAlbany)



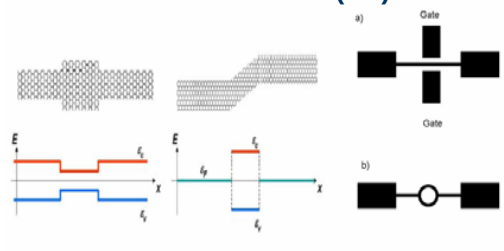
Single Electron Spin Devices
Raynolds et al (UAlbany)



Magnetoelectronic Devices
Multi bits logic Ross et al (MIT)



Graphene Nanowire Switches
Murali and DeHeer (GT)



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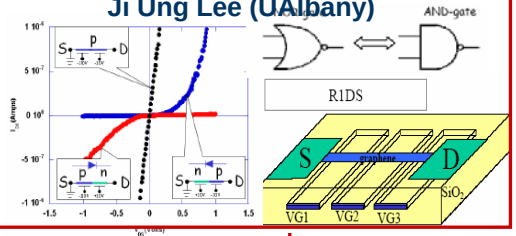
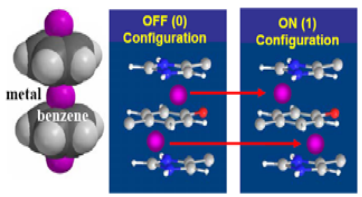
Post CMOS Switches

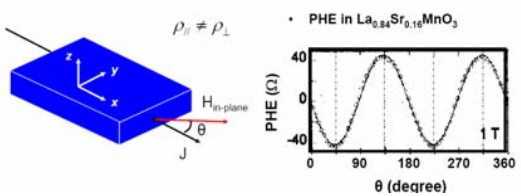
Reconfigurable One-Dimensional (1D) Switch (R1DS)
Ji Ung Lee (UAlbany)



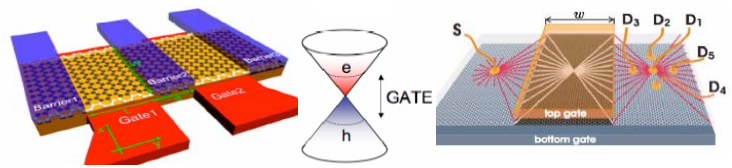
Molecular Nanowire Switches
Kaloyeros et al (UAlbany)



Logical Switches based on Complex Oxides
Ahn et al (Yale)



Graphene based Quantum Devices
Charles Marcus (Harvard)



Magnetic Quantum Cellular Automata (MQCA)

M. Niemier, Notre Dame

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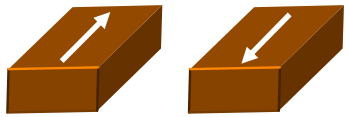
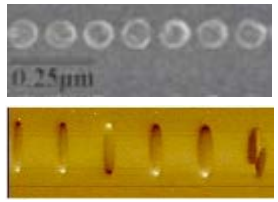
Schematic

Experimental

Device

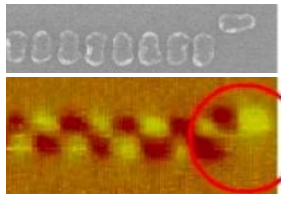




R. Cowburn, M. Welland, *"Room temperature magnetic quantum cellular automata,"* Science **287**, 1466, 2000

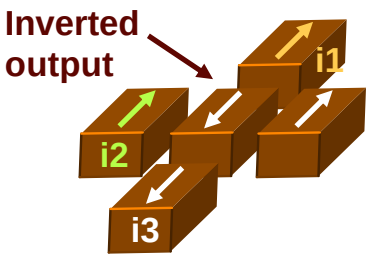
A. Imre, "Experimental Study of Nanomagnets for Magnetic QCA Logic Applications," U. of Notre Dame, Ph.D. Dissertation.

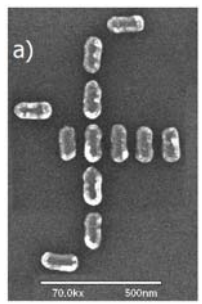
Wire

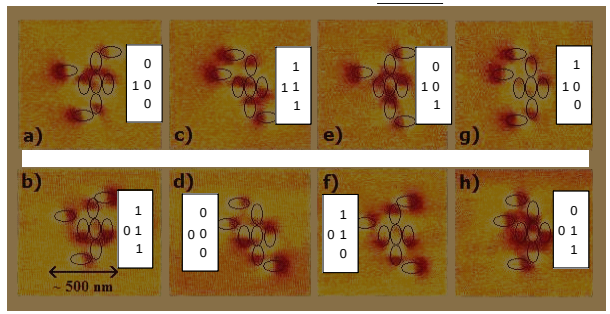


A. Imre, et. al., "Majority logic gate for Magnetic Quantum-Dot Cellular Automata," Science, vol. 311, No. 5758, pp. 205–208, January13, 2006.

Gate



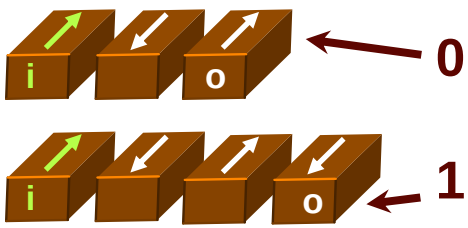




A. Imre, et. al. "Magnetic Logic Devices Based on Field-Coupled Nanomagnets," NanoGiga 2007.

A. Imre, et. al., "Majority logic gate for Magnetic Quantum-Dot Cellular Automata," Science, vol. 311, No. 5758, pp. 205–208, January13, 2006.

Inverter



2005 ITRS Energy / Cost / Area / Delay

Fig. 52, 2005 Emerging Research Devices Report www.itrs.net/reports.html

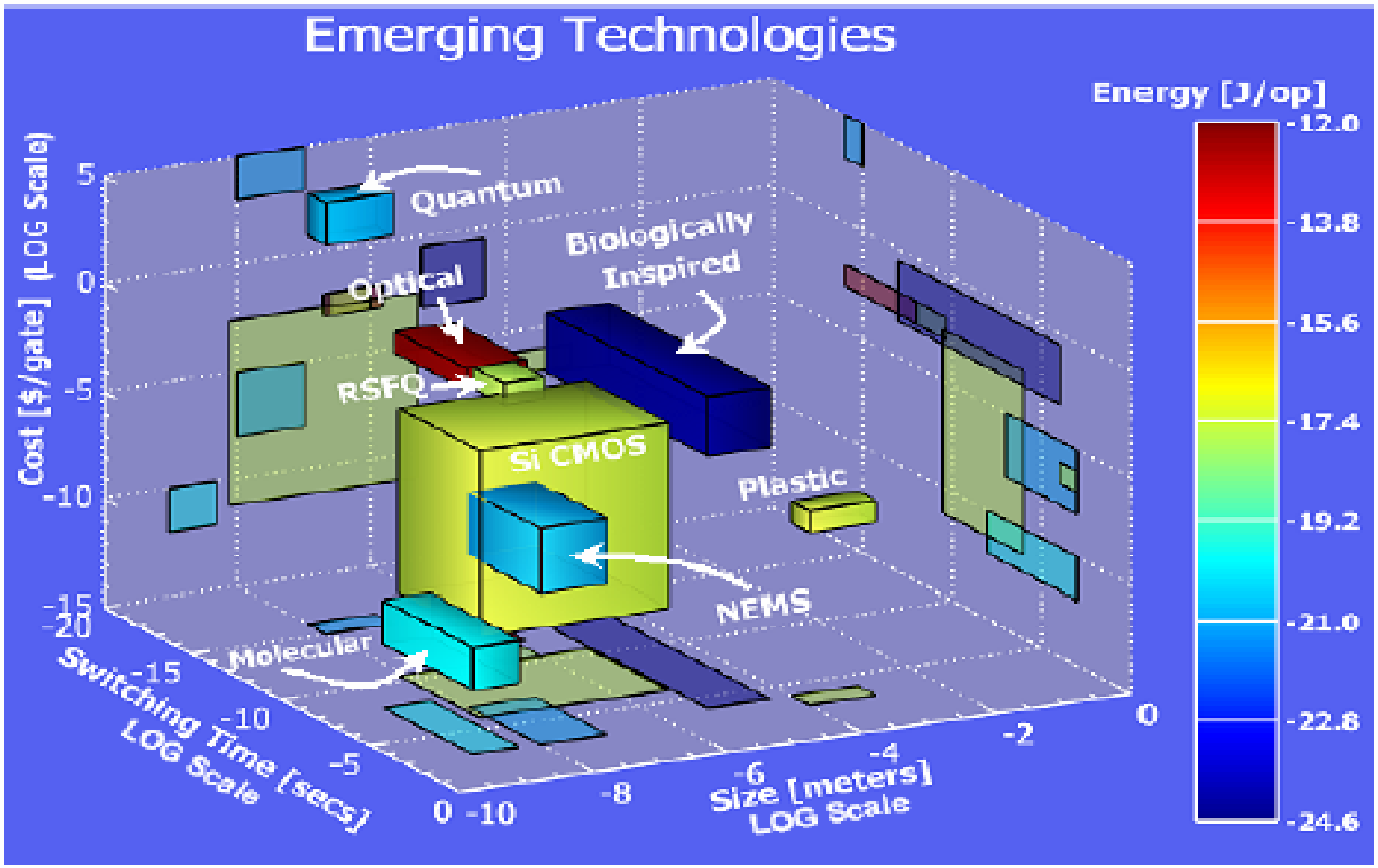
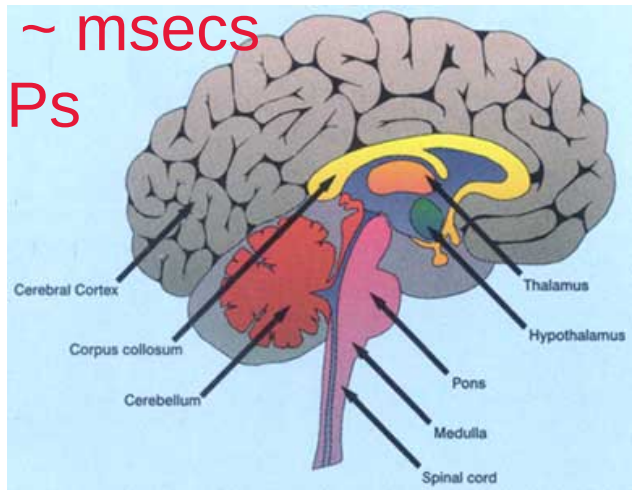


Figure 52 Parameterization of Emerging Technologies and CMOS—Speed, Size, Cost, and Switching Energy

Computing with Alternate State Variables

- Many different device ideas being considered – some 'likely' attributes compared to CMOS:
  - Slower
  - Denser / 3D
  - Local interconnect focused
  - Uniform arrays / sea-of-gates
  - Variability still an issue

'Switch' ~ msecs
~10^8 MIPs
~30W



Proof of concept?

- Architecture / System Question:
  - How to get high computation throughput with these attributes?

Two Take-aways

- Power will continue as the principal scaling issue for all IC applications
  - CMOS will continue to scale over at least the next decade, with emphasis on utilizing increasing transistor density over increasing frequency
- Any new technology must overcome the power / performance limits of a charge-based FET to continue the scaling trend of increased function / dollar
  - Does the device offer the prospect of lower energy storage / operation than CMOS?
  - Does the computation system offer the prospect of non-equilibrium or energy-recovery in operation?

Nanoelectronics Research Initiative

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