Roll Printing of Nanowires for Integrated Device and Sensor Arrays

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Fabrication of printable device and sensor arrays on bendable/flexible substrates may enable the development of a wide range of new technologies, including flexible displays, RF-ID tags, sensor tapes, artificial skin and more [1-7]. There has been a tremendous progress in this field over the past decade, mainly through the exploration of organic materials as the active semiconductor components. Overcoming the poor life-time and the low carrier mobility of these materials as compared to crystalline silicon; however, have been the major obstacles for achieving certain applications that require high speed, low power, and long lasting electronics [1-3]. Therefore, developing a new printable electronic materials technology with enhanced performance and stability is of large interest for the future progress of printable electronics. Recently, new methods for "printing" microscale and nanoscale inorganic structures have been proposed and developed. Unlike their organic counterparts, inorganic materials provide air stability while delivering high performances [4-15]. An example of such inorganic materials is crystalline semiconductor nanowires (NWs). In this paper, we review the recent advancements made in the assembly and integration of NW arrays on foreign substrates for device and sensor integration.

Crystalline Semiconductor Nanowires as Electronics Building Blocks

To date, a broad spectrum of functional nanowires have been synthesized, and successfully integrated as the building blocks of various single component device concepts, including transistors, sensors, optical diodes, NEMs, and more [4-15]. These chemically derived single-crystalline nanostructures (synthesized by chemical vapor deposition) present unique advantages over conventional semiconductors, as they enable integration of high-performance device elements onto virtually any substrate, including bendable plastics, with scaled on-currents and switching speeds comparable or higher than the state-of-the-art planar Si structures (depending on the specific NW material system). Particularly, high performance FETs based on high mobility InAs NWs have been recently demonstrated by multiple groups, exhibiting a high electron mobility of μ_n>2,000cm^2/Vs [15,12]. These high mobility NW materials present an ideal platform for attaining high performance printable electronics. Additionally, due to their miniaturized dimensions and large surface-area-to-volume ratio, NW sensors enable high spatial resolution and sensitivity. A major challenge facing the device/circuit integration of synthesized NWs is the controlled assembly on substrates with high uniformity over large areas. In recent years, multiple approaches have been explored for assembly of NWs on substrates with varying degree of success. Some of these alignment methods include liquid flow alignment, Langmuir-Blodgett technique, AC dielectrophoresis, blown bubble method, contact and roller printing, and more. In this article we report on the printing technology as a highly-efficient and scalable approach for ordered assembly of NW arrays on substrates for circuit integration.

Roll Printing of Nanowires on Substrates

We have recently developed a roll printing technology for the assembly of highly aligned NW arrays on various substrates [8-10]. The overall process involves (i) optimized growth of designed, crystalline NWs by nanocluster directed growth on a cylindrical substrate (i.e., roller), and (ii) patterned transfer of NWs directly from the roller to a receiver substrate via differential roll printing, as illustrated in Figure 1. After the growth of NWs, the roller is connected to a pair of wheels and brought into contact with the stationary receiver substrate, and rolled with a constant velocity [9]. An important aspect of this NW printing method is the mismatch of the roller and wheel radii (r_R, r_W, respectively) that results in a relative linear sliding motion of the roller relative to the stationary receiver substrate in addition to the rolling motion. This is different from traditional roll printing methods where such a mismatch would be undesirable since it would cause a distortion of the printed features. The relative sliding motion for $r_W \neq r_R$ generates the required directing field and shear force for the transfer of aligned NWs to the receiver substrate without which negligible density with random alignment is observed. Following the NW roll printing process, the patterned resist is removed by a standard lift-off process, leaving behind assembled NWs at the predefined locations. The process is highly generic for a wide range of NW materials, including Si, Ge, and compound semiconductors, and for the entire NW diameter range, d=10-100 nm, that has been explored. Furthermore, it is compatible with a wide range of rigid and flexible receiver substrates, including glass, Si, plastics, and paper (Fig. 2). This approach presents a highly scalable, low cost, and efficient method for assembling functional NWs on substrates, and may lead a revolutionary path toward the realization of high performance, flexible electronics based on printed single crystalline and high mobility nano-engineered materials.

The printed NW arrays are highly aligned in the direction of rolling and are limited to a monolayer (Fig. 3). To shed light on the transfer mechanism and the process dynamics, and to gain further control over the printing process, we have explored the role of surface chemical modification of the receiver substrate on the density of the printed NWs. For the $–CF_3$ terminated surfaces, we observed almost no transfer of NWs ($<10^{-3}$ NW/µm) from the donor to the receiver substrate while an identical printing process on –NH2 and $–N(Me)_3^+$ terminated monolayers resulted in a high density of transferred NWs, approaching ~8 NW/µm. Such a major density modulation of ~4 orders of magnitude demonstrates the key role of the surface interactions on the printing outcome. Fluorinated surfaces (i.e., $-CF_3$ terminated) are well known to be highly hydrophobic and "non-sticky", therefore, minimizing the adhesion of NWs to the receiver substrate during the sliding process. As a result, the wires remain rather unbroken on the donor substrate without being transferred to the receiver chip. On the other hand, $-NH_2$ and $–N(Me)_3^+$ terminated surfaces interact effectively with the NW surface to yield a high density transfer through strong bonding interactions. This demonstrates that during the printing process, NWs are dragged across a receiver substrate and are eventually detached from the roller as they are anchored to the surface functional groups of the receiver substrate by the van der Waals forces.

Printed Nanowire Arrays for Device Integration

After patterned printing of NW arrays on the receiver substrates, various device structures, including diodes and transistors, can be fabricated using conventional lithography methods with each device consisting of a parallel array of NWs. By tuning the width of the patterned regions for assembly, the ON current of the transistor can be readily modulated (Fig. 4) [8]. Importantly, by using parallel arrays of NWs as the active component of each device, the reliability and uniformity was significantly enhanced with σ~15% arising from the averaging effects [14].

Heterogeneous Assembly for Multi-Functional Circuit Integration

There is a tremendous interest to develop a versatile rout toward heterogeneous integration of crystalline materials on substrates for added functionality, for instance sensing capability, to conventional electronics. A unique feature of the NW printing technology, arising from its ambient temperature processing conditions, is that it enables for heterogeneous assembly of crystalline NWs on substrates for multi-functional circuit integration [10,14]. For instance, high mobility Ge NWs can be printed at certain locations on the receiver substrates to enable high performance transistors while optically active CdSe NWs (direct band gap, E_g~1.8eV) can be printed at other pre-defined sites to enable efficient photodetection [10]. This is in distinct contrast to the conventional Si processing for which the integration of crystalline compound semiconductors has proven to be quite challenging due to the lattice mismatch and interface problems. The fabrication of heterogeneous NW circuits involves a two-step printing of Ge and CdSe NWs at pre-defined locations on substrates followed by the device and circuit fabrication using conventional microfabrication processing. As a proof of concept, we have fabricated GeNW amplifiers and CdSe photodetectors that are integrated on-chip on rigid Si substrates (Fig. 5), demonstrating the feasibility of the NW printing technology for heterogeneous circuitry. The CdSe NW photodetectors were shown to be highly responsive to white light (~100x reduction in resistance upon irradiation to ~4 mW/cm^2) with the GeNW FETs amplifying the signal of the sensors by ~1000x. Owing to the uniformity of the printing process, a relatively large matrix (i.e. 13x20) of the all-NW sensor circuits were fabricated on a chip and utilized as an integrated imager (Fig. 6) [10]. This work not only demonstrates the NW device integration at an unprecedented scale, but also illustrates and presents a novel system based on printed NW arrays that may enable a number of technological applications utilizing NWs as the building blocks.

Conclusion

Significant progress has been made in the printing of NWs for highly ordered assembly of crystalline semiconductors on substrates with high uniformity. These parallel arrays of NWs are shows as high performance building blocks for diodes, transistors, and devices which can be readily integrated into functional circuits. Additionally, heterogeneous integration can be achieved using the proposed printing of NWs due to the ambient processing temperatures associated with this technology. The approach may enable a wide range of novel printable electronics, unattainable with conventional Si processing.

References

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Figure Captions:

Figure 1. Differential roll printing of NWs. (a), Schematic of the DRP setup. (b), Optical photograph of the assembled apparatus used in this work (top view). The inset shows the blank and NW coated glass tubes used as the rollers (I and II, respectively). Obtained with permission from [9]. Copyright AIP 2007.

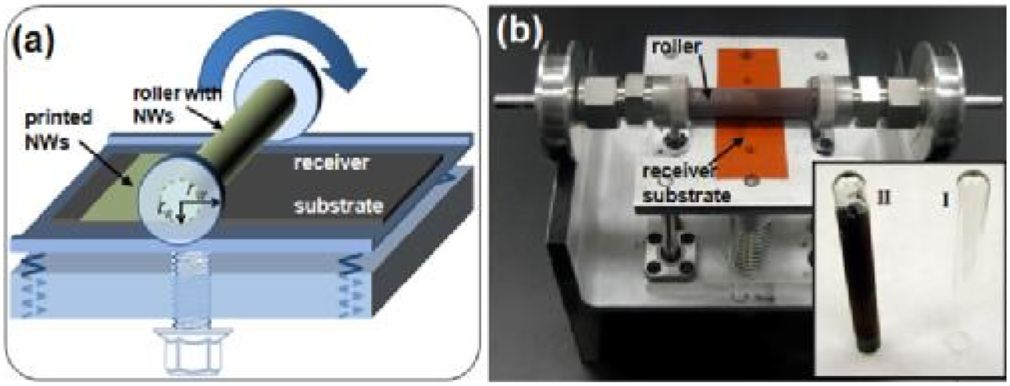
Figure 2. Printed NW arrays on unconventional substrates: glass and paper (L) and plastic (R). Refer to Figure 3 for high magnification images of the printed NW arrays. Obtained with permission from [9]. to Figure 3 for high magnification images of the printed NW arrays. Copyright 2007 AIP.

Figure 3. Optical and SEM (left middle) images of printed Ge NW arrays. The printed NWs are ~30 nm in diameter. [8]

Figure 4. Devices based on printed NW arrays. (a) From top to bottom, SEM images of back-gated single GeNW FET, 10 µm and 250 µm wide parallel arrayed NW FETs. (b) ON current as a function of channel width scaling, showing a highly linear trend. Obtained with permission from [8]. Copyright 2008 ACS.

Figure 5. Heterogeneous NW assembly for an all integrated, sensor circuitry. (A) Circuit diagram for the all-NW photodetector, with high mobility Ge/Si NW FETs (T1 and T2) amplifying the photoresponse of a CdSe nanosensor. (B) Schematic of the all-NW optical sensor circuit based on ordered arrays of Ge/Si and CdSe NWs. (C1) An optical image of the fabricated NW circuitry, consisting of a CdSe nanosensor [NS, (C2)] and two Ge/Si core/shell NW FETs [T2 and T1, (C3)-(C4)] with channel widths ~300 µm and 1 µm, respectively. Each device element within the circuit can be independently addressed for dynamics studies and circuit debugging.

Figure 6. Schematic of an array of NW sensor circuitry with imaging functionality.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roller with NWs
printed NWs
receiver
substrate
(b)
roller
receiver substrate
II
I

Figure 1

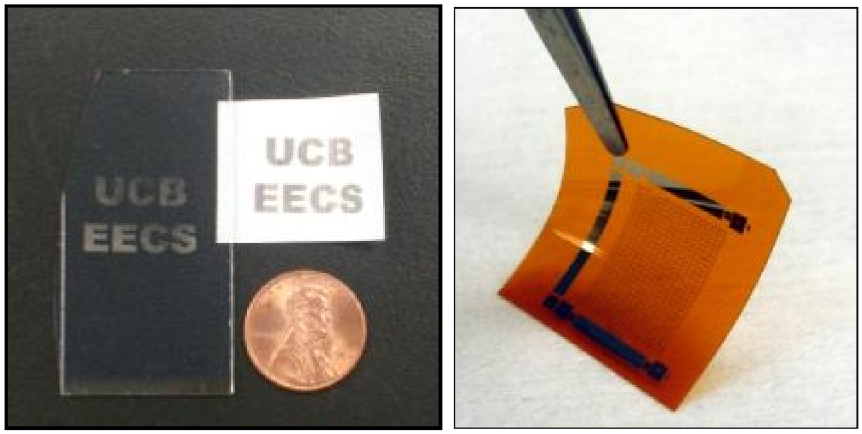

Figure 2

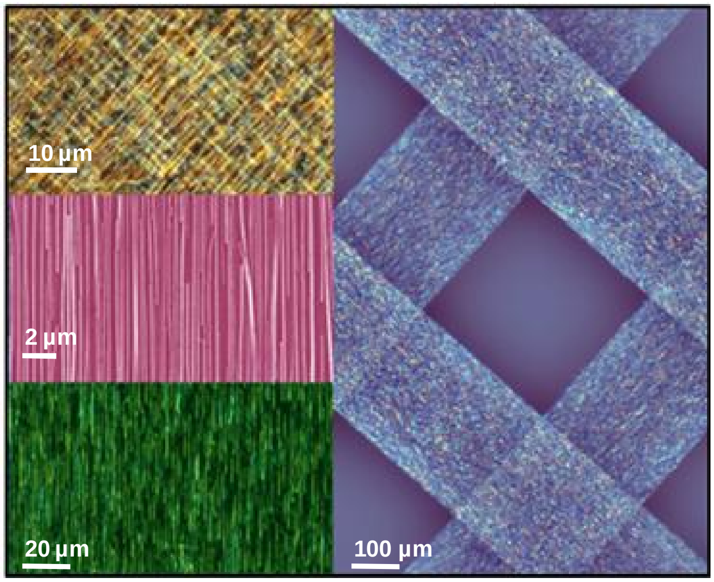

Figure 3

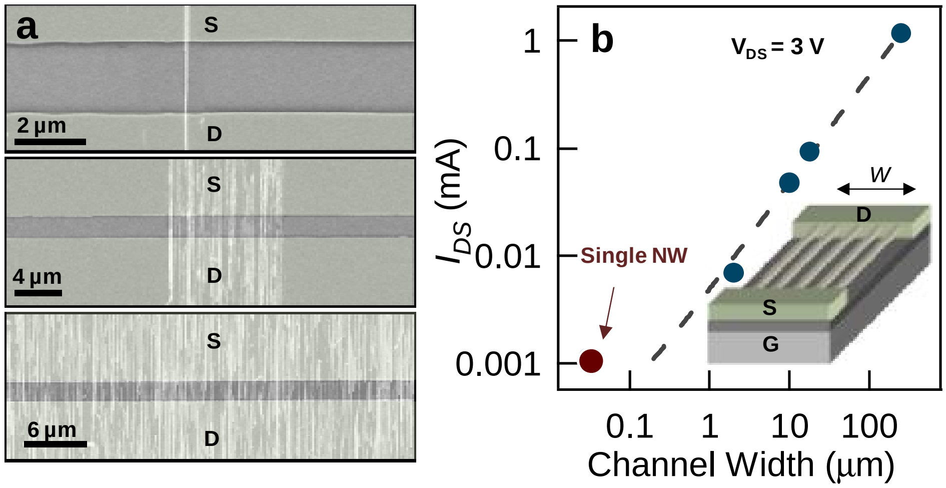
a
S
2 μm
D
S
4 μm
D
S
6 μm
D
b
V_{DS} = 3 V
W
D
S
G
Single NW
I_{DS} (mA)
1
0.1
0.01
0.001
0.1
1
10
100
Channel Width (μm)

Figure 4

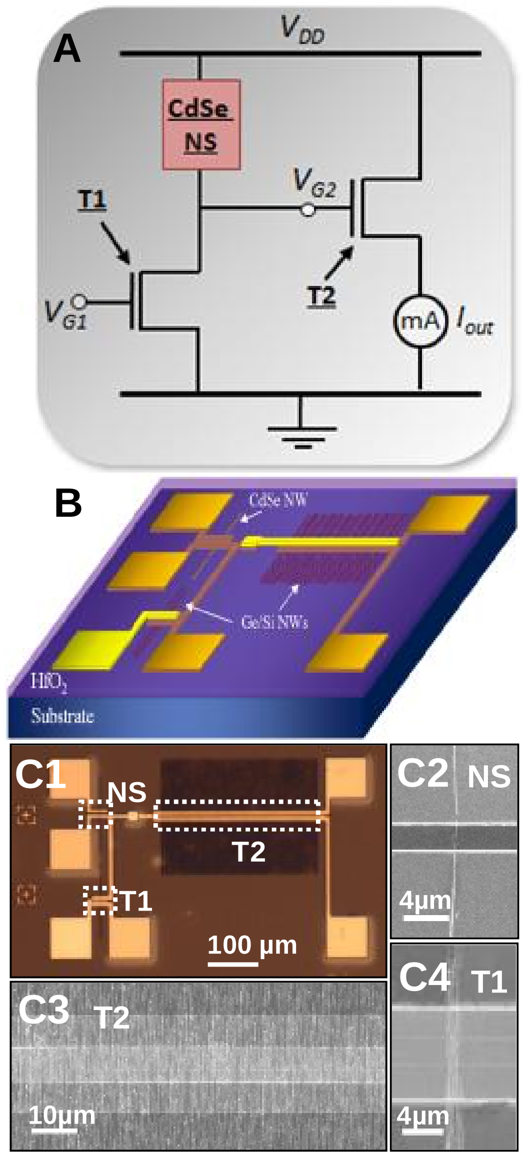
A
V_{DD}
CdSe NS
T1
V_{G2}
T2
V_{G1}
mA
I_{out}
B
CdSe NW
Ge/Si NWs
HfO_2
Substrate
C1
NS
T2
T1
100 µm
C2
NS
4µm
C3
T2
10µm
C4
T1
4µm

Figure 5

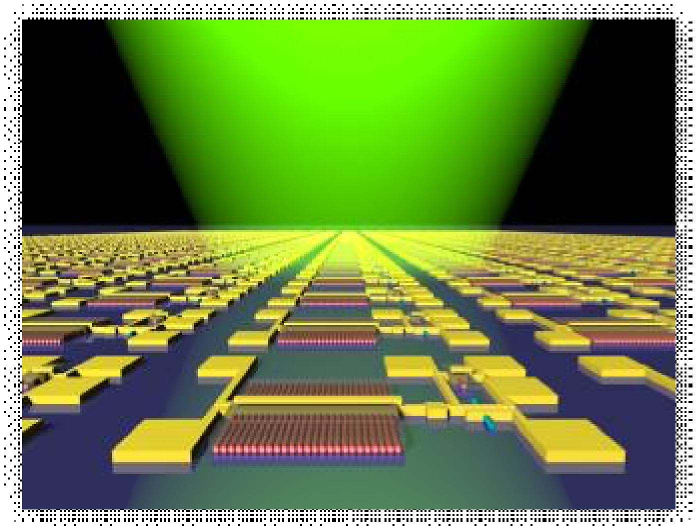

Figure 6