Integration of III-V Optoelectronics and Si-photonics: New Developments and Application Opportunities

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The tremendous miniaturization of integrated circuits has been the driving force for the latest industrial revolution and the emergence of information-driven economy. Conventional scaling approaches based on Si-microelectronics have hit technology limitations for speed of data transfer and power consumption. In particular, downscaling of integrated circuits (IC) has allowed a continuous increase of the functionality of everyday electronic equipment and deployment of tremendous communication and computation capabilities, for example in the form of large data centers. However, the on-chip power consumption has become one of the greatest limitations of the current computation technology and emergence of new device architectures are crucial to achieving future performance increase required, for example, to ensure the massive data traffic generated by the usage of social media and cloud services.

Key to making this happen is the use of light-based technology, more specifically in the form of photonic integrated circuits (PICs), which refers broadly to a technology platform that allows the combination of different optical components, such as lasers, modulators and photodetectors, on a single chip. PICs can allow optical systems to be made more compact and achieve higher performance than using discrete optical components yet for many practical applications they should share a common fabrication technology with microelectronic chips. In particular, the possibility to integrate III-V technology (used in optoelectronics for light emitting devices) with Si-based technology would enable to merge the two major information technology platforms: photonics and electronics. Breakthrough in this area is instrumental for increasing the data processing and transfer rate and simultaneously reduce the electrical power. Moreover, integration of III-V/Si platforms is a major avenue for development of integrated sensors with increased functionality that will revolutionize the way we are interacting with environment.

With this perspective in mind, the presentation will review two major approaches for the integration of microelectronics and optoelectronics technologies. As a first approach, we will discuss progress concerning the use of silicon photonics and hybrid integration with III-V optoelectronic components. Silicon photonics enables extremely dense integration of passive optical components and shares same fabrication processes with CMOS microelectronics technology. On the other hand, Si lacks the ability to provide efficient light sources, a function which is rendered possible by III-V optoelectronics. Leading developments in this field in Finland are concerned with the use of silicon-on-insulator (SOI) technology employing large waveguides in which the optical mode field is almost completely confined inside the SOI core. In turn, this leads to small propagation losses, small polarization dependency and good tolerance to high optical powers and processing imperfections. Furthermore, the use of thick rib waveguides can provide single-mode functionality over an ultra-wide wavelength range (from 1.2 μm to >2 μm). Detailed developments of III-V optoelectronics chips for hybrid integration on SOI will be reviewed emphasizing the challenges that have been recently tackled to make the integration

process feasible for practical application. For example, we have recently focused on developing III-V-chips with better dimensional control, alignment marks and novel waveguide geometries. Another area of developments to be emphasized is concerned with deployment of GaInNSbAs/GaAs as an optoelectronic platform for active chips and its use in semiconductor optical amplifiers and modulators integrated on SOI. For example, we have demonstrated GaInNSbAs SOAs able to provide gain at 1300-1550 nm wavelength band with improved thermal behaviour compared to InP-based components typically employed for hybrid integration at this wavelength range. In addition, GaAs-based wafers have better scalability to volume compared to InP. At the application level we will present several implementations based on SOI/III-V hybrid integration platform for 100Gb/s optical transceivers to be deployed in data-centres [1]. Moreover, a novel concept of programmable light source for spectroscopy at 3 μm wavelength range will be also introduced [2]. The developments have been part of major EU research programs.

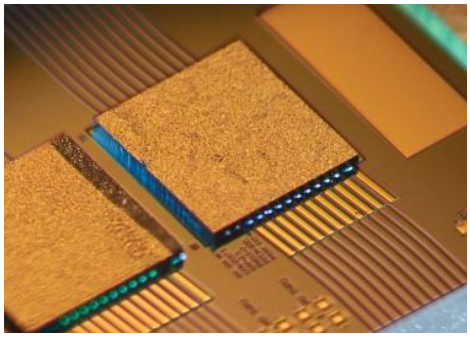

Fig. 1. *Example of a hybrid integrated circuits including 11 GaInNAs-based SOAs mounted on SOI (picture courtesy of Timo Aalto, VTT).*

The second area of developments outlined is concerned with emerging PICs technology employing direct integrating of III-V alloys on Si by heteroepitaxy. In this case, the main challenge is related to different lattice constants and crystal structures between the III-V and Si, resulting in formation of threading dislocations and antiphase boundaries. One of the most promising ways to overcome these problems is to grow the III-V material on Si as thin, one-dimensional structures, referred to as nanowires (NWs). III-V NWs grown on Si do not suffer from lattice or thermal mismatch because of the small interface area between the NWs and the substrate crystal. To this end we will review recent results concerning catalyst-free of ordered NWs with excellent control of their length and size [3]. Their use as light sources employing new concepts for coupling to Si waveguides will be introduced.

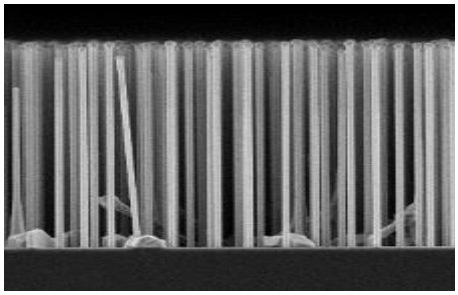

Fig. 2. *Ordered GaAs nanowires epitaxially grown on Si with lithography-free oxide patterns.*

References

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2. http://www.h2020-miregas.eu
3. T. Hakkarainen, A. Schramm, J. Mäkelä, P. Laukkanen, and M. Guina "Lithography-free oxide patterns as templates for self-catalyzed growth of highly uniform GaAs nanowires on Si(111)" Nanotechnology, Vol. 26, Nr. 27 (2015)